IN THE CLAIMS:

Please accept amended claims 1 and 4 and new claims 8-10 as follows:

1. (currently amended) A thin film transistor array panel comprising:

a substrate;

a gate electrode;

a gate insulating layer formed on the gate electrode;

a polysilicon layer formed on the gate insulating layer and including a pair of ohmic contact areas doped with conductive impurity;

source and drain electrodes formed on the ohmic contact areas at least in part;

a storage conductor formed on the gate insulating layer overlapping a portion of a gate line formed on the substrate;

a passivation layer formed on the source and the drain electrodes and having a first contact hole exposing the drain electrode at least in part and a second contact hole exposing the storage conductor; and

a pixel electrode formed on the passivation layer and connected to the drain electrode and the storage conductor through the first contact hole and the second contact hole, respectively.

2. (original) The thin film transistor array panel of claim 1, wherein the conductive impurity comprises boron or phosphorous.

3. (original) The thin film transistor array panel of claim 1, wherein concentration of the impurity ranges from about 1×10^{14} to about 1×10^{16}.

4. (currently amended) The thin film transistor array panel of claim 1, ~~further comprising: a~~ wherein the gate line is disposed between the substrate and the gate insulating layer and is connected to the gate electrode; and the thin film transistor array panel further comprises a data line disposed between the gate insulating layer and the passivation layer and connected to the source electrode.

5. (original) A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate electrode;

depositing a gate insulating layer and a polysilicon layer on the gate electrode in sequence;

forming a photoresist having a first portion and a second portion thinner than the first portion on the polysilicon layer;

patterning the polysilicon layer using the photoresist as a mask to form a semiconductor layer;

removing the second portion of the photoresist;

performing impurity implantation using the first portion of the photoresist as a mask to form ohmic contact areas in the semiconductor layer;

removing the first portion of the photoresist;

forming source and drain electrodes on the ohmic contact areas;

forming a passivation layer having a contact hole on the drain electrode; and

forming a pixel electrode on the passivation layer.

6. (original) The method of claim 5, wherein the formation of the photoresist comprising:

coating a photoresist film on the polysilicon layer;

exposing the photoresist film through a photo-mask having a slit pattern or a translucent portion facing the second portion of the photoresist; and

developing the photoresist film to form the photoresist.

7. (original) The method of claim 5, wherein the impurity comprises p type conductive impurity.

8. (new) The method of claim 5, wherein the first portion of the photoresist is positioned over a middle portion of the gate electrode and the second portion of the photoresist is positioned over end portions of the gate electrode.

9. (new) The method of claim 8, wherein the second portion of the photoresist is further positioned over areas adjacent to the end portions of the gate electrode.

10. (new) A method of manufacturing a thin film transistor array panel, the method comprising:

forming a gate electrode;

depositing a gate insulating layer and a polysilicon layer on the gate electrode in sequence;

forming a photoresist having a first portion and a second portion thinner than the first portion on the polysilicon layer, wherein the first portion of the photoresist is positioned over a middle portion of the gate electrode and the second portion of the photoresist is positioned over end portions of the gate electrode,

patterning the polysilicon layer using the photoresist as a mask to form a semiconductor layer;

removing the second portion of the photoresist;

performing impurity implantation using the first portion of the photoresist as a mask to form ohmic contact areas in the semiconductor layer; and

removing the first portion of the photoresist.